VRM 8.2 DC–DC Converter Design Guidelines

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Applications and terminology

This document defines a range of DC-to-DC converters to meet the power requirements of computer systems using Intel microprocessors. It does not attempt to define a specific voltage regulator module (VRM) implementation. VRM requirements will vary according to the needs of different computer systems, including the range of processors a specific VRM is expected to support in a system. The "VRM" designation may refer to a voltage regulator on a system board, as well as to the module defined in Section 2.

The VRM 8.2 definition is specifically intended to meet the needs of Intel® Celeron™, Pentium® II, and Pentium III processor-based systems, although its features may be applicable to some Pentium II Xeon™ and Pentium III Xeon processor-based systems with appropriate power distribution paths. See *VRM 8.3 DC-DC Converter Design Guidelines* for a VRM definition specifically directed toward multiple-processor systems.

Each guideline is placed into one of three categories. The category immediately follows the section heading and is one of the following:

REQUIRED: An essential part of the design—necessary to meet processor voltage and current specifications.

EXPECTED: Part of Intel's processor power definitions; necessary for consistency with the designs of many systems and power devices.

PROPOSED: Normally met by of this type of DC-to-DC converter and, therefore, included as a design target. Likely to be specified by system manufacturers.

1. Electrical Specifications

1.1 Output Requirements

REQUIRED

The Voltage Regulator Module (VRM) supplies the required voltage and current to a processor as shown in the following tables.

The following conditions apply to the specifications:
- Specifications apply to all frequencies unless specific frequencies are listed.
- Icc_{CORE} is measured at nominal Vcc_{CORE} under maximum signal loading conditions.

Table 1, Voltage and Current Specifications for 2.8–Volt Pentium® II Processors

Symbol	Parameter	Processor core frequency (MHz)	Minimum	Typical	Maximum	Unit
Vcc_{CORE}	Vcc for processor core (measured at VRM pins)			2.8		V
	Vcc_{CORE} static tolerance at processor connector pins on system board		–0.060		0.100	V
	Vcc_{CORE} transient tolerance at processor connector pins on system board	233 266 300	–0.140 –0.140 –0.130		0.140 0.140 0.130	V
Icc_{CORE}	Current for Vcc_{CORE}	233 266 300		6.9 7.8 8.7	11.8 12.7 14.2	A
Icc_{SGNT}CORE	Icc for Stop-Grant Vcc_{CORE}	233 266 300		0.8 0.9 1.0	1.1 1.2 1.3	A
$dIcc_{CORE}/dt$	Icc slew rate				30	A/µs

Maximum Icc_{CORE} measurement note (applies to Tables 1-5) — Voltage regulators may be designed with a minimum equivalent internal resistance to ensure that the output voltage, at maximum current output, is no greater than the nominal (i.e., typical) voltage level of Vcc_{CORE} ($Vcc_{CORE–TYP}$). In this case the maximum current level for the regulator ($Icc_{CORE–REG}$) can be reduced from the specified maximum Icc_{CORE} ($Icc_{CORE–MAX}$) and is calculated by the equation:

$$Icc_{CORE–REG} = Icc_{CORE–MAX} \times (Vcc_{CORE–TYP} - Vcc_{CORE} \text{ static tolerance}) / Vcc_{CORE–TYP}$$

For example, a VRM supporting the 300 MHz Pentium II processor could be designed for:

$$Icc_{CORE–REG} = 14.2 \times (2.8 - 0.06) / 2.8 = 13.9 \text{ A}$$

Table 2, Voltage and Current Specifications for 2.0–Volt Pentium® II (D) and Pentium® III (K) Processors

Symbol	Parameter	Processor core frequency (MHz)	Minimum	Typical	Maximum	Unit
Vcc_{CORE}	Vcc for processor core			2.0		V
	Vcc_{CORE} static tolerance at VRM pins on system board	(D) 333 (D) 350-450 (K) 450-500	–0.060 –0.060 –0.060		0.100 0.070 0.070	V
	Vcc_{CORE} transient tolerance at VRM pins on system board	(D) 333 (D) 350-450 (K) 450-500	–0.110 –0.100 –0.130		0.110 0.100 0.130	V
	Vcc_{CORE} static tolerance at processor connector pins on system board	(D) 333 (D) 350-450 (K) 450-500	–0.070 –0.070 –0.070		0.100 0.070 0.070	V
	Vcc_{CORE} transient tolerance at processor connector pins on system board	(D) 333 (D) 350-450 (K) 450-500	–0.120 –0.110 –0.140		0.120 0.110 0.140	V
Icc_{CORE}	Current for Vcc_{CORE}	(D) 333 (D) 350 (D) 400 (D) 450 (K) 450 (K) 500			10.6 11.1 12.6 14.2 14.5 16.1	A
$Icc_{SGNT}CORE$	Icc for Stop-Grant Vcc_{CORE}				0.8	A
$dIcc_{CORE}/dt$	Icc slew rate				20	A/µs

Table 3, Voltage and Current Specifications for Intel® Celeron™ Processors

Symbol	Parameter	Processor core frequency (MHz)	Min	Typical	Max	Unit
Vcc_{CORE}	Vcc for processor core			2.0		V
	Vcc_{CORE} static tolerance at processor connector pins on system board		–0.089		0.100	V
	Vcc_{CORE} transient tolerance at processor connector pins on system board		–0.144		0.144	V
Icc_{CORE}	Current for Vcc_{CORE}	300A 333 366 400			9.2 10.1 11.2 12.2	A
$Icc_{SGNT}CORE$	Icc for Stop-Grant Vcc_{CORE}				0.8	A
$DIcc_{CORE}/dt$	Icc slew rate				20	A/µs

Table 4, Processor Support by VRM Type

VRM Type	Processors Supported
(VRM 8.1)	*Pentium® II processor, 233-333 MHz*
VRM 8.2–1	Pentium® II processor, 233-400 MHz
VRM 8.2–2	VRM 8.2-1, plus Pentium® II processor at 450 MHz (2.0V Vcc_{CORE})
VRM 8.2–3	VRM 8.2-2, plus Pentium® III processor at 450 MHz (2.0V Vcc_{CORE})
VRM 8.2–4	VRM 8.2-3, plus Pentium® III processor at 500 MHz (2.0V Vcc_{CORE})
VRM 8.2–11	Intel® Celeron™ processor at 300-400 MHz (2.0V Vcc_{CORE})

♦ Static Voltage Regulation — REQUIRED

The output voltage measured at the VRM output pins on the system board must be within the static range shown in the respective tables, except for input voltage turn-on and turn-off and for current transitions as shown under "Transient Voltage Regulation" below. The static limits apply to ambient temperatures between 0°C and 60°C. Static voltage regulation includes:

- DC output initial voltage set point adjust
- Output ripple and noise
- Output load ranges specified in tables above
- Temperature and warm up specified in Section 3.1.

♦ Transient Voltage Regulation — REQUIRED

The output voltage measured at the VRM output pins on the system board must be within the transient range shown in the respective tables, including the transition from $Icc_{SGNTCORE}$ (Stop-Grant state) to Icc_{CORE} (Maximum) or from Icc_{CORE} (Maximum) to $Icc_{SGNTCORE}$ (Stop-Grant state), except as noted for input voltage turn-on and turn-off. This tolerance must include the variation due to DC voltage regulation plus the effects of the output load transient at the VRM output pins. Vcc_{CORE} during a load transient response may be outside of the static voltage specifications for no longer than 100 µsec. The toggle rate for the output load transition must range from 100 Hz to 100 kHz. Under the above conditions and for all toggle rates, the transient response must be measured over a 20 MHz frequency band, and at ambient temperatures between 25°C and 50°C.

♦ Output Ripple and Noise — PROPOSED

Ripple and noise are defined as periodic or random signals over a 20 MHz frequency band at the output pins under constant load. Output ripple should be consistent with the static voltage requirements.

♦ Variation with Load — PROPOSED

To assist in providing margin during high-slew-rate current load transitions, the VRM output may have a positive offset (≤40 mV) under minimum load conditions, and a negative offset (≤40 mV) under maximum load conditions.

♦ Turn-on Response Time — PROPOSED

The output voltage should be within its specified range within 10 msec of the input reaching 95% of its nominal voltage.

♦ **Overshoot at Turn-On or Turn-Off** **REQUIRED**

Overshoot upon the application or removal of the input voltage under the conditions specified in Section 1.2 must be less than 10% above the initial set output voltage. No negative voltage may be present on any output during turn-on or turn-off.

♦ **Power Good Output—PWRGD** **EXPECTED**

An open collector signal consistent with TTL DC specifications should be provided This signal should transition to the open (>100KΩ) state within 20 milliseconds of the input stabilizing within the range specified in Section 1.2. The signal should be in the low-impedance (to ground) state whenever Vout is more than ±12% from nominal and be in the open state whenever Vcc_{CORE} is within its specified range.

Some systems logically combine power good signals from multiple processors and reset all processors if any processor's Vcc_{CORE} source fails. Other systems use VID codes for voltages below 1.8V for identification purposes. Such systems may require the VRM's PWRGD output to be in the high state when the VRM's Vcc_{CORE} output is disabled by VID inputs, including the no-processor code (11111). That is,

PWRGD = (Vcc_{CORE} outputs within 12% of nominal) OR (output disabled in response to VID code).

1.2 Input Voltage and Current

♦ **Input Voltages** **EXPECTED**

Available inputs are at 12V ±5% and 5V ±5%. Any single voltage or combination may be used by the VRM. These voltages are supplied by a conventional computer power supply through a cable to the motherboard. Input voltage requirements should be clearly marked on the module.

♦ **Load Transient Effects on Input Voltages** **PROPOSED**

The VRM should be able to provide for an output current step at the load from Icc_{CORE} (Stop-Grant state) to Icc_{CORE} (Maximum) or Icc_{CORE} (Maximum) to Icc_{CORE} (Stop-Grant state) within the time interval listed in Section 1.1. During this step response the input current di/dt should not exceed 0.1A/µsec. For applications with multiple VRMs on any voltage source on a board, the step response di/dt of an individual VRM should not exceed 0.04A/ µsec.

1.3 Input Controls

These are signals that control the VRM (shown with corresponding pins in Figure 2).

♦ **Output Enable—OUTEN** **EXPECTED**

The VRM should accept an open collector signal consistent with TTL DC specifications for controlling the output voltage: The logic low state disables the output voltage.

♦ **Voltage Identification—VID[0:4]** **EXPECTED**

The VRM should accept five signals, used to indicate the voltage required by the processor, as defined by Table 5. Five processor package pins have an open–ground pattern corresponding to the voltage required by the individual processor unit. Some system designs may use pull-up resistors to pull open VID lines to a TTL V_{IH} level. Generally these pull-ups will use the VRM input voltage, with an appropriate resistor divider if the input voltage is 12 volts. If used, such pull-ups should have a resistance ≥ 10KΩ.

Table 5, Voltage Identification Code

Processor Pins 0 = Connected to Vss 1 = Open or pull-up to Vin					Vcc_{CORE}	Processor Pins 0 = Connected to Vss 1 = Open or pull-up to Vin					Vcc_{CORE}
VID4	VID3	VID2	VID1	VID0	(VDC)	VID4	VID3	VID2	VID1	VID0	(VDC)
0	1	1	1	1	1.30	1	1	1	1	1	No CPU
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

Note: Table shows the full VID range for reference. Vcc_{CORE} requirements are:

1.8V–2.8V for full range of Pentium® II processors

1.8V–2.05V for Pentium® II and Pentium® III processors

1.3V–2.05V for Intel® Celeron™ processors

1.4 Efficiency

PROPOSED

The efficiency of the VRM should be greater than:

- 80% at maximum output current
- 40% at 0.5A.

1.5 Protection

These are features built into the VRM to prevent damage to itself or the circuits it powers.

♦ Over Voltage Protection **PROPOSED**

Protection Level: The VRM should provide over-voltage protection by shutting itself off when the output voltage rises beyond Vtrip. Vtrip should be set between 110% and 125% of the nominal voltage demanded by the processor (via the VID pins).

Voltage Sequencing: No combination of input voltages should falsely trigger an OVP event.

♦ **Short Circuit Protection** **PROPOSED**

Load short circuit is defined as a load impedance of less than approximately 90 mΩ. The VRM should be capable of withstanding a continuous short-circuit to the output without damage or over-stress to the unit.

♦ **Reset After Shutdown** **PROPOSED**

If the VRM goes into a shutdown state due to a fault condition on its outputs, the VRM should return to normal operation after the fault has been removed, or after the fault has been removed and power has been cycled off and on.

1.6 Current Sharing

PROPOSED

The pin designated Ishare is intended to permit two or more VRMs to balance the total current load between them. There is no expectation of interoperability between the sharing mechanisms of different module or system implementations.

2. Module Requirements

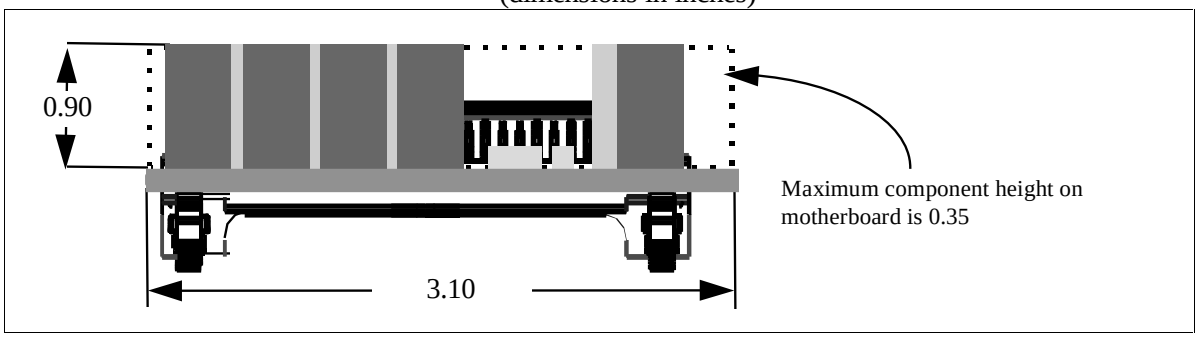
The VRM 8.2 interface should be mechanically compatible with Intel's Voltage Regulator Module Header 8, revision 3.0. For detailed voltage regulator module, connector, and header dimensions, see: Intel application note AP-523, *Pentium® Pro Processor Power Distribution Guidelines*, Order Number: 242764.

♦ **Dimensions** **EXPECTED**

Outline dimensions should be equal to or less than 3.1" x 1.5" x 1.1". Maximum component height should be 0.90" on the connector side and 0.14" on the back side of the module.

Figure 1, Module Top View

(dimensions in inches)



♦ Interconnect **EXPECTED**

Interconnect should consist of a 40 pin interface, type AMPMOD2 or equivalent, with the socket (part number 532956-7 or equivalent) mounted to the module. The current capacity must be at least 2A/pin. The pin electrical interface should be as shown in Table 6.

♦ Mating header (reference)

The VRM 8.2 Header is a 40-position, two-row shrouded header with straight posts on 0.1 inch centers (ref. AMP # 146315-1 or equivalent). The voltage regulator module is to be retained to and removed from the header by features on the header that mate with the voltage regulator module. The removal and installation process must not require the use of tools. The removal features must be accessible from the back side (opposite the receptacle) of the module (ref. Figure 1).

♦ Weight **EXPECTED**

Package weight, including any integral heat sink, should be less than three ounces.

♦ Marking **EXPECTED**

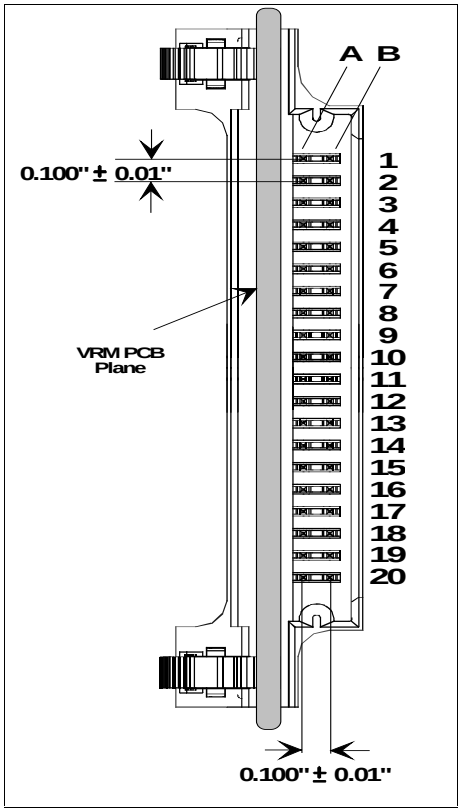
The input voltage (either +5VDC or +12VDC) should be conspicuously marked on the module, to be visible during insertion of the module into the header. Marking options include:

– Color code the text on the label: red = +5V; blue = +12V.
– List the output voltage range and input and output currents.

Table 6, Module Pinout

Pin #	Row A	Row B
1	5Vin	5Vin
2	5Vin	5Vin
3	5Vin	5Vin
4	12Vin	12Vin
5	12Vin	Reserved
6	Ishare	OUTEN
7	VID0	VID1
8	VID2	VID3
9	VID4	PWRGD
10	Vcc_{CORE}	Vss
11	Vss	Vcc_{CORE}
12	Vcc_{CORE}	Vss
13	Vss	Vcc_{CORE}
14	Vcc_{CORE}	Vss
15	Vss	Vcc_{CORE}
16	Vcc_{CORE}	Vss
17	Vss	Vcc_{CORE}
18	Vcc_{CORE}	Vss
19	Vss	Vcc_{CORE}
20	Vcc_{CORE}	Vss

Figure 2, Pin Orientation



3. Module Tests and Standards

PROPOSED

3.1 Environmental

Design, including materials, should be consistent with the manufacture of units that meet the environmental reference points in Table 7.

Table 7, Environmental Specifications

	Operating	Non-Operating
Temperature	Ambient 0°C to +60°C at full load with a maximum rate of change of 5°C/10 minutes minimum but no more than 10°C/hour. [1]	Ambient –40°C to 70°C with a maximum rate of change of 20°C/hour. [2]
Humidity	To 85% relative humidity.	To 95% relative humidity.
Altitude	0 to 10,000 feet	0 to 50,000 feet.
Electrostatic discharge	15 KV initialization level. The direct ESD event shall cause no out-of-regulation conditions. [3]	25 KV initialization level.

[1] See Section 1.2 for static and transient test conditions.

[2] Thermal shock of –40°C to +70°C, 10 cycles; transfer time shall not exceed 5 minutes, duration of exposure to temperature extremes shall be 20 minutes.

[3] Includes overshoot, undershoot, and nuisance trips of the over-voltage protection, over-current protection or remote shutdown circuitry.

3.2 Shock and Vibration

The VRM should not be damaged and the interconnect integrity not compromised during:

- A shock of 50G with an 11 millisecond half sine wave, non-operating, the shock to be applied in each of the orthogonal axes.
- Vibration of $0.01G^2$ per Hz at 5 Hz, sloping to $0.02G^2$ per Hz at 20 Hz and maintaining $0.02G^2$ per Hz from 20 Hz to 500 Hz, non-operating, applied in each of the orthogonal axes.

3.3 Electromagnetic

Design, including materials, should be consistent with the manufacture of units that comply with the limits of FCC Class B and VDE 243 Level B for radiated emissions, given the existence of an external package around the VRM with 20dB of shielding.

3.4 Reliability

The VRM should be designed to function to electrical specifications, within the environmental specifications, with 60°C air at a velocity of 100 LFM directed along the connector axis.

♦ **Component De-rating**

The following component de-rating guidelines should be followed:

- Semiconductor junction temperatures should be < 115°C with ambient at 50°C.
- Capacitor case temperature should not exceed 80 % of rated temperature.
- Resistor wattage de-rating should be consistent with the resistor type.
- Component voltage and current de-rating should be > 20%, the effects of ripple current heating should be accounted for in this de-rating.

♦ **Mean-Time-Between-Failures (MTBF)**

Design, including materials, should be consistent with the manufacture of units with an MTBF of 500,000 hours of continuous operation at 55°C, maximum-outputs load, and worst-case line, while meeting specified requirements. MTBF should be calculated in accordance with MIL-STD-217F (parts stress method).

3.5 Safety

Design, including materials, should be consistent with the manufacture of units that meet the standards of UL flammability specifications per 94V-0.

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